IN THE CLAIMS

The following claims are pending in the present application:

1. (Original) A substrate of an integrated circuit package, comprising:

a base structure having upper and lower sides and a plurality of via openings formed therein;

a conductive via in each via opening, the conductive vias including at least power and ground vias; and

first and second capacitor structures on the upper and lower sides of the base structure respectively, each capacitor structure including conductive power and ground planes and a dielectric layer between the power and ground planes, the power and ground planes being electrically connected to at least one of the power and ground vias, respectively.

2. (Original) The substrate of claim 1, wherein the base structure is made of a sintered ceramic material.

3. (Original) The package substrate of claim 1, wherein the vias include signal vias, each signal via being electrically disconnected from both the power and ground planes.

4. (Original) The substrate of claim 3, wherein the dielectric layer of the

capacitor structure is made of a dielectric material with a high k-value, the substrate having first and second portions, the first portion having the high k-value dielectric material and the second portion not having the high k-value dielectric material, the signal vias being formed in the second portion.

5. (Original) An integrated circuit package, comprising:

a base structure having upper and lower sides and a plurality of via openings formed therein;

a conductive via in each via opening, the conductive vias including at least power and ground vias; and

first and second capacitor structures on the upper and lower sides of the base structure respectively, each capacitor structure including conductive power and ground planes and a dielectric layer between the power and ground planes, the power and ground planes being electrically connected to at least one of the power and ground vias, respectively; and

a die having an integrated circuit formed therein mounted on the substrate.

6. (Original) The integrated circuit package of claim 5, wherein the substrate is an interposer substrate, further comprising:

a package substrate, the interposer substrate being mounted to the package substrate.

7. (Original) The integrated circuit package of claim 6, wherein the vias are connected to contacts on the package substrate without an x-y transformation.

8. (Original) The integrated circuit package of claim 5, wherein the vias include signal vias, each signal via being electrically disconnected from both the power and ground planes.

9. (Original) The integrated circuit package of claim 8, wherein the dielectric layer of the capacitor structure is made of a dielectric material with a high k-value, the substrate having first and second portions, the first portion having the high k-value dielectric material and the second portion not having the high k-value dielectric material, the signal vias being formed in the second portion.

10. (Original) A method of constructing at least a portion of an integrated circuit package, comprising:

forming a base structure having first and second opposing sides and a plurality of via openings therein;

forming a conductive via in each via opening of the base structure, the conductive vias including at least power and ground vias; and

forming first and second capacitor structures on the first and second sides, respectively, of the base structure, each capacitor structure including conductive power and ground planes and a dielectric layer between the power and ground

planes, the power and ground planes being electrically connected to at least one of the power vias and one of the ground vias, respectively.

11. (Original) The method of claim 10, wherein the vias include signal vias, each signal via being electrically disconnected from both the power and ground planes of both capacitor structures.

12. (Original) The method of claim 11, wherein the dielectric layer of the capacitor structure is made of a dielectric material with a high k-value, the substrate having first and second portions, the first portion having the high k-value dielectric material and the second portion not having the high k-value dielectric material, the signal vias being formed in the second portion.

13. (Original) A method of constructing at least a portion of an integrated circuit package, comprising:

forming a base structure, of a green material, having first and second opposing sides and a plurality of via openings therein;

sintering the green material so that the green material becomes a sintered ceramic material and the base structure becomes a sintered ceramic base structure having the via openings;

forming a conductive via in each via opening of the sintered ceramic base structure, the conductive vias including at least power and ground vias; and

forming first and second capacitor structures on the first and second sides, respectively, of each sintered ceramic base structure, the capacitor structure including conductive power and ground planes and a dielectric layer between the power and ground planes, the power and ground planes being electrically connected to at least one of the power vias and one of the ground vias, respectively.

14. (Original) The method of claim 13, wherein the vias include signal vias, each signal via being electrically disconnected from both the power and ground planes of both capacitor structures.

15. (Original) The method of claim 14, wherein the dielectric layer of the capacitor structure is made of a dielectric material with a high k-value, the substrate having first and second portions, the first portion having the high k-value dielectric material and the second portion not having the high k-value dielectric material, the signal vias being formed in the second portion.

16. (Original) The method of claim 13, wherein the vias are connected to contacts on the sintered ceramic base structure without an x-y transformation.

SUMMARY

Applicant believes that the above remarks are fully responsive to the Office Action dated November 16, 2004. If the Examiner has any questions, Applicant respectfully requests that the Examiner contact the undersigned by telephone at (408) 720-8300.

DEPOSIT ACCOUNT AUTHORIZATION

Please charge any shortages and credit any overages to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: December 16, 2004

Stephen M. De Klerk
Reg. No. 46,503

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8300